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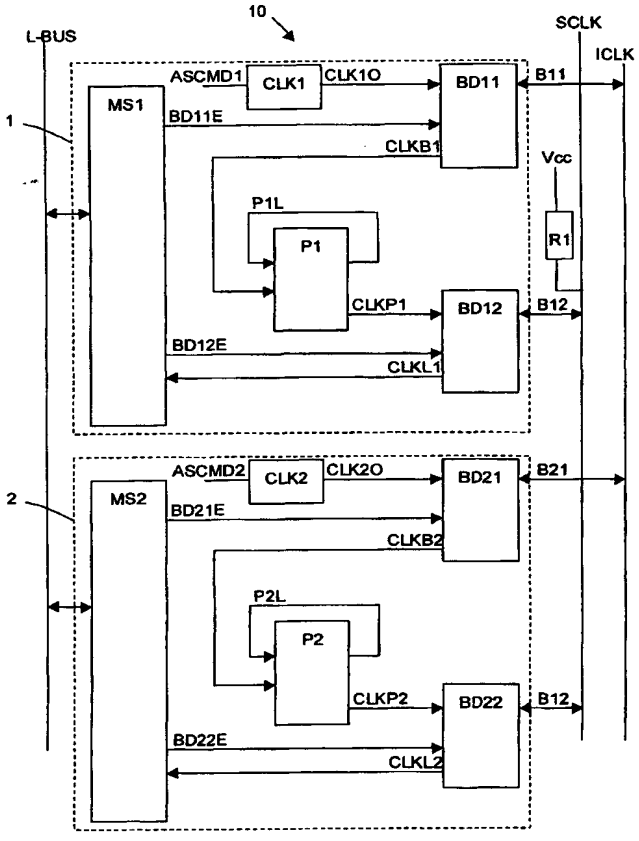
(54) Title: SEAMLESS CLOCK



(57) Abstract: System (10) comprising at least two units (1, 2) with clock functionality, the units being coupled to a common system clock line (SCLK), a common internal clock line (ICLK), and a logic bus (L-BUS), whereby one sole unit (1, 2) is being dedicated as a mater unit at a time. One source clock signal (CLK10, CLK20) of a unit is output on the internal clock line (ICLK) and all PLL devices of all units generates PLL output signals derived from the internal clock signal, the outputs of the PLL devices (CLKP1, CLKP2) being in phase with one another such that switchover from one PLL output signal to another is seamless.

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